PENDING CLAIMS:

Claims 1–76 (Canceled).

77. (Previously Presented) An integrated circuit structure, comprising:

a substrate;

a field oxide over the substrate, the field oxide having an opening therethrough to a surface of the substrate;

a gate electrode over the surface of the substrate and within the opening, the gate electrode having insulating material on a bottom and on two sides of the gate electrode, wherein the insulating material on the bottom of the gate electrode contacts the substrate; and

source and drain regions within the substrate and adjacent the insulating material on sides of the gate electrode, each source and drain region including

a first portion in the substrate, and

a second portion on the substrate over the first portion and adjacent to the insulating material on the sides of the gate electrode,

wherein the first and second portions together function as a source or drain for a device including the gate electrode.

78. (Previously Presented) The integrated circuit structure of claim 77, wherein the opening through the substrate has substantially vertical sidewalls.

79. (Previously Presented) The integrated circuit structure of claim 78, wherein each source and drain region is formed between a sidewall of the opening and the insulating material on the sides of the gate electrode.

80. (Previously Presented) The integrated circuit structure of claim 79, wherein a space between a sidewall of the opening and the insulating material on the sides of the gate electrode is filled with material forming the second portion of one of the source and drain regions.

81. (Previously Presented) The integrated circuit structure of claim 77, further comprising:

LDD regions for the source and drain regions formed within the first portion of each source and drain region.

82. (Previously Presented) The integrated circuit structure of claim 81, wherein the LDD regions are formed in the substrate beneath the insulating material on the sides of the gate electrode.

83. (Previously Presented) The integrated circuit structure of claim 77, wherein the gate electrode, the insulating material on the sides of the gate electrode, and the second portions of the source and drain regions fill a space between sidewall spacers on sidewalls of the opening.

84. (Previously Presented) The integrated circuit structure of claim 77, an upper surface of the gate electrode is further from a surface of the substrate than an upper surface of the field oxide.

85. (Previously Presented) The integrated circuit structure of claim 77, wherein the first and second portions of the source and drain regions are both formed of a semiconductor material doped to include lightly doped regions within at least the first portions and heavily doped regions within at least the second portions.

86. (Previously Presented) The integrated circuit structure of claim 77, wherein the second portions of the source and drain regions each form contact regions for source/drain contacts.

87. (Previously Presented) The integrated circuit structure of claim 82, wherein the LDD regions are the first portions of the source and drain regions.

88. (Previously Presented) The integrated circuit structure of claim 77, wherein the second portions of the source and drain regions have a dopant concentration suitable for heavily doped source/drain regions.

89. (Previously Presented) The integrated circuit structure of claim 88, wherein the dopant concentration within the second portions of the source and drain regions is formed by implanting dopants at a dosage of approximately 6×10^{15} at 40 KeV.

90. (Previously Presented) The integrated circuit structure of claim 88, wherein the LDD regions are the first portions of the source and drain regions.

91. (Previously Presented) The integrated circuit structure of claim 88, wherein the first portions of the source and drain regions include the LDD regions and portions of heavily doped source and drain regions.

92. (Previously Presented) The integrated circuit structure of claim 77, further comprising:

a refractory metal silicide on the second portions of the source and drain regions include the LDD regions and portions of heavily doped source and drain regions.

93. (Previously Presented) An integrated circuit structure, comprising:

a field oxide over a substrate, the field oxide having an opening therethrough to a surface of the substrate;

a gate structure on the surface of the substrate within the opening, the gate structure having insulating material on a bottom and sides of a gate electrode forming a gate oxide between the gate electrode and a source region and between the gate electrode and a drain region;

doped regions within portions of the substrate within the opening which are adjacent to and extend beneath the gate structure, wherein the doped regions within the substrate are at least lightly doped; and

doped semiconductor material on the substrate within the opening adjacent to the gate structure and over each of the doped regions within the substrate, the doped semiconductor material doped to a concentration suitable for heavily doped source and drain regions,

wherein each of the doped regions within the substrate and the overlying doped semiconductor material form, and together function as, either the source region or the drain region for a transistor including the gate structure.

94. (Previously Presented) The integrated circuit structure of claim 93, wherein the doped semiconductor material on the substrate has a dopant concentration formed by implanting dopants at a dosage of approximately 6×10^{15} at 40 KeV.

95. (Previously Presented) The integrated circuit structure of claim 93, wherein an upper surface of the doped semiconductor material is coated with a refractory metal silicide to form a contact region to the source and drain.

96. (Previously Presented) A transistor, comprising:

a gate electrode on an insulating layer over a substrate surface;

insulating sidewall layers on the gate electrode; and

doped source and drain regions within portions of the substrate adjacent to and extending beneath the insulating sidewall layers and within semiconductor material on the substrate adjacent to the insulating sidewall layers,

wherein the portions of the source and drain regions within the substrate are at least lightly doped and the portions of the source and drain regions within the semiconductor material on the substrate are doped to a concentration suitable for heavily doped source and drain regions,

wherein the portion of the source region within the substrate and the portion of the source region within the semiconductor material on the substrate together function as a source for the transistor, and

wherein the portion of the drain region within the substrate and the portion of the drain region within the semiconductor material on the substrate together function as a drain for the transistor.